REMARKS

Claim Rejections under 35 U.S.C. 102

Claims 1-5 and 7-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Hiramatsu et al. (U.S. Pat. 5,311,040).

Hiramatsu (FIG. 1) discloses a thin film transistor comprising: a substrate (1, 3); a gate electrode 2 made of Ta or MoTa disposed in the substrate (column 3, lines 25-26); and a gate silicon nitride insulation layer 4 disposed on the substrate and gate electrode (column 3, lines 30-32).

Amended claim 1 now recites in pertinent part "a thin film transistor, comprising: a substrate; **a gate electrode disposed in the substrate**; [and] a gate insulation layer disposed on the substrate and the gate electrode."

Applicant now traverses the rejection insofar as it applies to amended claim 1, as follows:

Hiramatsu (FIG. 1) discloses that "[a] gate electrode 2 having a thickness of 200 nm and made of a Ta film or an MoTa alloy film **is formed on a light-transmitting insulating substrate 1** made of a glass substrate. A silicon oxide film 3 serving as a first gate insulating film and having a thickness of about 300 nm is formed on the substrate 1 to cover the gate electrode 2" (column 3, lines 25-30).

Thus, amended claim 1 recites a gate electrode **disposed in the substrate**, and

Hiramatsu (FIG. 1) discloses a gate electrode 2 **covered by a first gate insulating film formed on the substrate 1**. Since the substrate of amended claim 1 is different from the first gate insulating film of Hiramatsu, and the meaning of "disposed in" is different from that of "covered by," these differences indicate that Hiramatsu does not teach a thin film transistor comprising all the limitations recited in amended claim 1.

Further, applicant submits that claim 1 is patentable over Hiramatsu under 35 U.S.C. 103. There is nothing in the cited reference that teaches or suggests to one of ordinary skill in the art that they might or should provide the thin film transistor of amended claim 1. Moreover, the thin film transistor of amended claim 1 produces new and unexpected results. That is, **the gate electrode is deposited in the substrate**, and thus the thickness of the gate electrode can be changed by changing the depth of the substrate etched. As a result, it is easy to increase the thickness of the gate electrode to reduce its impedance, so that the thin film transistor of amended claim 1 can efficiently reduce an RC delay of a scanning signal.

Accordingly, amended claim 1 is submitted to be patentable over Hiramatsu. Reconsideration and withdrawal of the rejection and allowance of amended claim 1 are respectfully requested.

Claims 2-5 and 7-10 depend either directly or indirectly from independent amended claim 1, and therefore should also be allowable.

For similar reasons to those asserted above in relation to amended claim 1, it is submitted that Hiramatsu does not disclose, teach or suggest all the limitations of

the thin film transistor of the display device recited in amended claim 11.

Accordingly, amended claim 11 is submitted to be patentable over Hiramatsu under both 35 U.S.C. 102(b) and 35 U.S.C. 103. Reconsideration and withdrawal of the rejection and allowance of amended claim 11 are respectfully requested.

Claim Rejections under 35 U.S.C. 103

Claims 6 and 21 are understood to be rejected under 35 U.S.C. 103(a) as being unpatentable over Hiramatsu. (U.S. Pat. 5,311,040) in view of Vu et al. (U.S. Pat. 5,702,963).

Examiner states that Hiramatsu does not disclose a substrate defining a cavity in an upper face and a gate electrode filled in the cavity.

Examiner further states that Vu (FIGS. 15D-15E) teaches a substrate 1054 defining a cavity 1062 in an upper face and a gate electrode filled in the cavity; and that accordingly, it would have been obvious to form the gate electrode of Hiramatsu by defining a cavity in the substrate because such forming of the cavity would permit the forming of the gate electrode in a backside region of the substrate, as taught by Vu (column 3, lines 54-60).

Claim 21 now recites in pertinent part "[a] thin film transistor comprising: **a substrate defining a cavity in an upper surface; [and] a gate electrode filled in said cavity**."

Applicant now traverses the rejection insofar as it applies to amended claim 21,

as follows:

Firstly, the thin film transistor of claim 21 comprises, inter alia, a substrate defining a cavity in an upper face, a gate electrode filled in said cavity, a gate insulation layer applied upon said substrate covering both said substrate and said gate electrode.

Vu (FIGS. 15D and 15E), discloses "after single transfer, using an opposite polarity gate mask (not shown) the oxide layer 1054 is thinned down to a few hundred angstroms along the channel region 1062...the oxide layer along the channel region 1062 is etched away to expose the backside of the device 1050. Next, a thin oxide layer 1063 ... can be deposited in the region 1062. **A second gate (G2) is then formed over the thin oxide layer 1063** and electrically connected to the first gate (G1)..." (column 15, lines 6-17).

Thus, claim 21 specifies that **a cavity is defined in an upper face of the lowest substrate, and the gate electrode is filled in the cavity**. However, in Vu, the channel region 1062 is defined in the oxide layer 1054, which is not the lowest substrate 1060, and **the second gate is then formed over the thin oxide layer 1063 deposited in the region 1062**. Since the position of the cavity claimed in claim 21 is different from that of the region 1062 disclosed in Vu, the position of the gate electrode claimed in claim 21 is different from that of the second gate disclosed in Vu. Therefore combining the cavity of Vu with Hiramatsu would not teach or suggest the thin film transistor of claim 21, since the cavity of Vu is not the same as that of claim 21.

Secondly, in claim 21, the gate electrode is filled in the cavity defined in the

upper face of the substrate, and then the thickness of the gate electrode can be changed by changing the depth of the cavity. As a result, it is easy to increase the thickness of the gate electrode to reduce its impedance, so that the thin film transistor of claim 21 can efficiently reduce an RC delay of a scanning signal.

By contrast, in Vu, the second gate is positioned on the opposite side of the plane of the silicon island as the first gate over the channel region, and a contact is then attached to the second gate, and the two gates can then be electrically connected. Further, a three-dimensional MOSFET device is formed. The usage and advantages of Vu are different from those of claim 21. Therefore, when Vu is combined with Hiramatsu, it would not have obvious to obtain the present invention with its unique advantages.

In summary, there is nothing in the cited reference that teaches or suggests to one of ordinary in the art that they might or should be combined to provide the thin film transistor of claim 21. Moreover, the thin film transistor of claim 21 produces new and unexpected results.

Accordingly, claim 21 is submitted to be patentable over Hiramatsu in view of Vu. Reconsideration and withdrawal of the rejection and allowance of claim 21 are respectfully requested.

Claim 6 depends directly from amended claim 1. Applicant refers to and relies on the above-detailed assertions of the patentability of claim 1 over Hiramatsu. There is nothing in Vu, when considered together with Hiramatsu, that provides any additional teaching or suggestion to one of ordinary skill in the art that they might or should provide the thin film transistor of claim 1.

Accordingly, because claim 6 depends from claim 1, claim 6 is submitted to be patentable over Hiramatsu in view of Vu. Reconsideration and withdrawal of the rejection and allowance of claim 6 are respectfully requested.

In view of the foregoing, the present application as claimed in the pending claims is considered to be in a condition for allowance, and an action to such effect is earnestly solicited.

Respectfully submitted,
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(NH-X^4-C=O):	X^4 = c) L-azetidine-2-carboxylic acid
(NH-X^5-C=O):	X^5 = b) D-tyrosine
(NH-X^6-C=O):	X^6 = g) L-homoarginine
Y^2:	Y^2 = b) an amino group (the carboxylic acid group in the C-terminal amino acid is replaced by an amide group).

This election of species reads on all claims in Group IV (claims 91, 117, 118, and 124). Applicants make these elections of species to be fully responsive to the species election requirement.

Pursuant to MPEP section 809.02(a) upon allowance of a generic claim, Applicants will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. Accordingly, Applicants submit that upon allowance of the generic claims, all the remaining non-elected claims must be considered.

Therefore, in view of the above amendments and remarks, it is respectfully requested that the application be reconsidered and that all pending claims be allowed and the case passed to issue.

If there are any other issues remaining which the Examiner believes could be resolved through either a Supplemental Response or an Examiner's Amendment, the Examiner is respectfully requested to contact the undersigned at the telephone number indicated below.

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Respectfully submitted,

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Amendments to the Drawings:

The replacement sheet of drawings includes a change to FIG. 14. The new FIG. 14 has the additional caption "PRIOR ART."

Attachment: Replacement Sheet